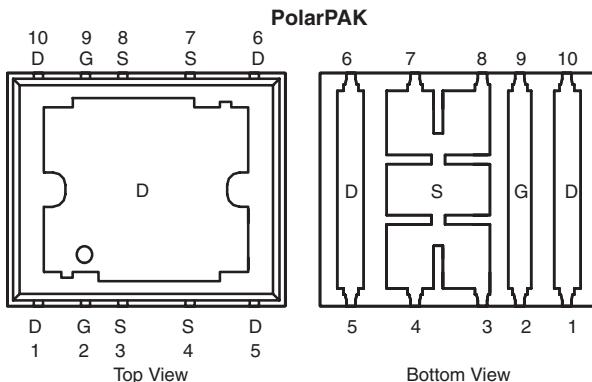


## N-Channel 20-V (D-S) MOSFET

### PRODUCT SUMMARY

V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>		Q <sub>g</sub> (Typ.)
		Silicon Limit	Package Limit	
20	0.00117 at V <sub>GS</sub> = 10 V	258	60	45 nC
	0.0016 at V <sub>GS</sub> = 4.5 V	220	60	

Package Drawing

[www.vishay.com/doc?72945](http://www.vishay.com/doc?72945)

Top surface is connected to pins 1, 5, 6, and 10

Ordering Information: SiE874DF-T1-GE3 (Lead (Pb)-free and Halogen-free)

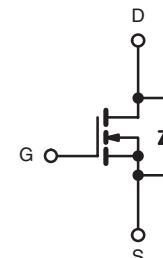
### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Gen III Power MOSFET
- Ultra Low Thermal Resistance Using Top-Exposed PolarPAK® Package for Double-Sided Cooling
- Leadframe-Based New Encapsulated Package
  - Die Not Exposed
  - Same Layout Regardless of Die Size,  $\leq 100$  V
- Low Q<sub>gd</sub>/Q<sub>gs</sub> Ratio Helps Prevent Shoot-Through
- 100 % R<sub>g</sub> and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



### APPLICATIONS

- POL
- OR-ing
- DC/DC



N-Channel MOSFET

For Related Documents

[www.vishay.com/ppg?65350](http://www.vishay.com/ppg?65350)

### ABSOLUTE MAXIMUM RATINGS T<sub>A</sub> = 25 °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	20	V
Gate-Source Voltage	V <sub>GS</sub>	$\pm 20$	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	258 (Silicon Limit)	
		60 <sup>a</sup> (Package Limit)	
		60 <sup>a</sup>	
		52 <sup>b, c</sup>	
		42 <sup>b, c</sup>	
Pulsed Drain Current	I <sub>DM</sub>	100	
Continuous Source-Drain Diode Current	I <sub>S</sub>	60 <sup>a</sup>	
		4.3 <sup>b, c</sup>	
Single Pulse Avalanche Current	I <sub>AS</sub>	40	
Avalanche Energy	E <sub>AS</sub>	80	mJ
Maximum Power Dissipation	P <sub>D</sub>	125	
		80	
		5.2 <sup>b, c</sup>	
		3.3 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260	

Notes:

- Package limit is 60 A.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- See Solder Profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

## SiE874DF

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## THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a, b</sup>	Steady State	$R_{thJA}$	20	24	°C/W
Maximum Junction-to-Case (Drain Top)		$R_{thJC}$ (Drain)	0.8	1	
Maximum Junction-to-Case (Source) <sup>a, c</sup>		$R_{thJC}$ (Source)	2.2	2.7	

Notes:

- a. Surface Mounted on 1" x 1" FR4 board.
- b. Maximum under Steady State conditions is 68 °C/W.
- c. Measured at source pin (on the side of the package).

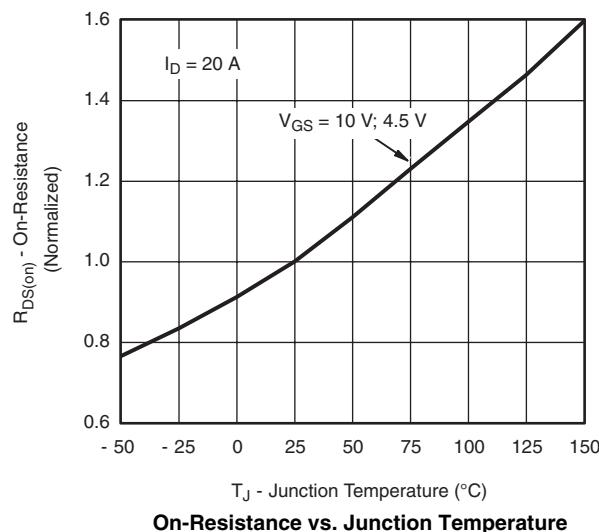
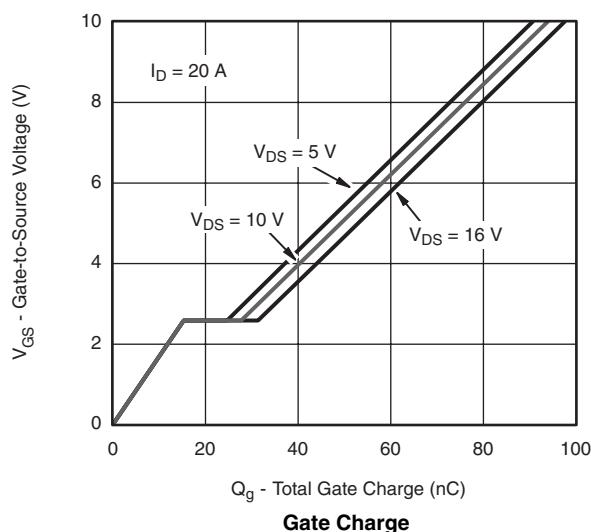
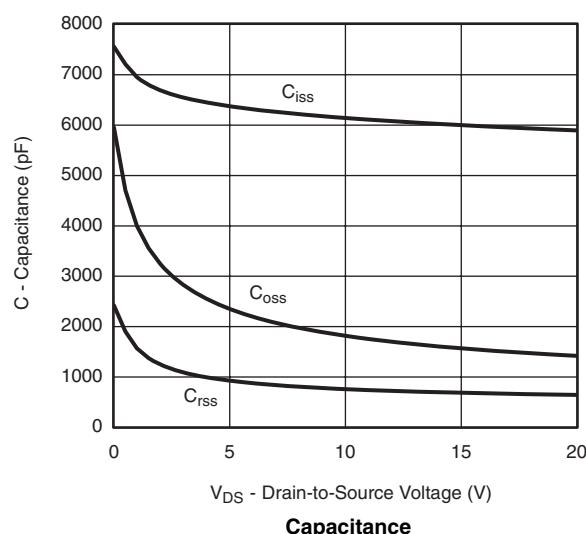
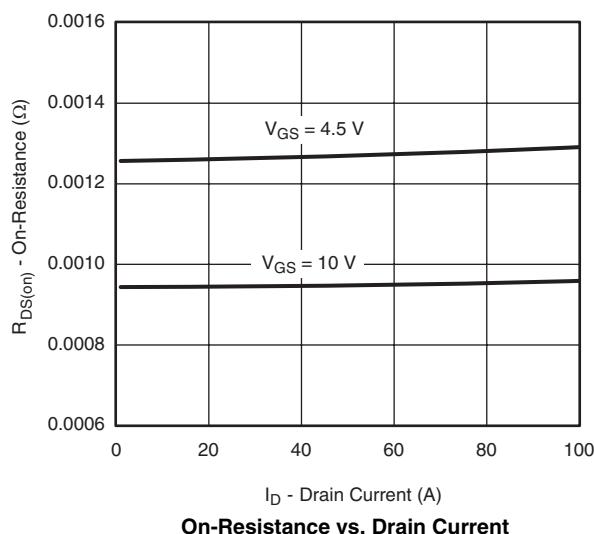
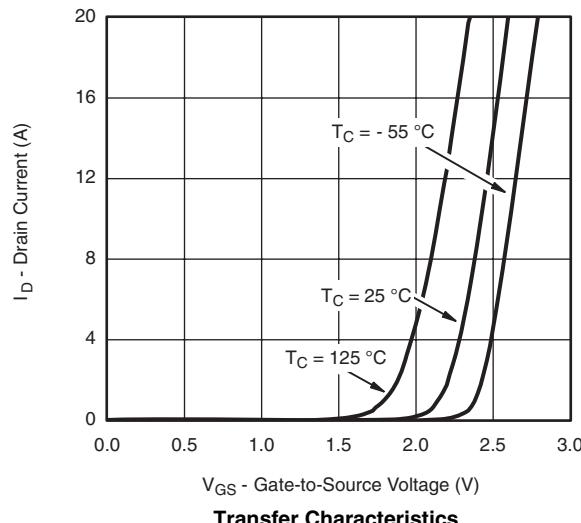
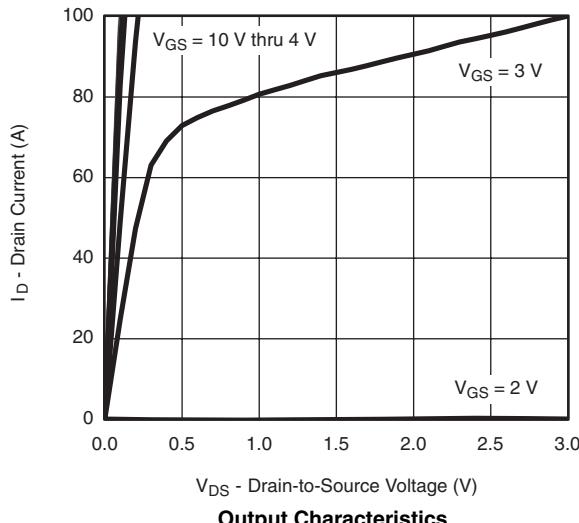
SPECIFICATIONS  $T_J = 25^\circ\text{C}$ , unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}$ , $I_D = 250 \mu\text{A}$	20			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \mu\text{A}$		20		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 6.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$	1.0	1.7	2.2	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}$ , $V_{GS} = \pm 20 \text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 20 \text{ V}$ , $V_{GS} = 0 \text{ V}$			1	μA
		$V_{DS} = 20 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 55^\circ\text{C}$			10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5 \text{ V}$ , $V_{GS} = 10 \text{ V}$	25			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$ , $I_D = 20 \text{ A}$		0.00095	0.00117	Ω
		$V_{GS} = 4.5 \text{ V}$ , $I_D = 20 \text{ A}$		0.0013	0.0016	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15 \text{ V}$ , $I_D = 20 \text{ A}$			110	S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 10 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $f = 1 \text{ MHz}$		6200		pF
Output Capacitance	$C_{oss}$			1800		
Reverse Transfer Capacitance	$C_{rss}$			760		
Total Gate Charge	$Q_g$	$V_{DS} = 10 \text{ V}$ , $V_{GS} = 10 \text{ V}$ , $I_D = 20 \text{ A}$		95	145	nC
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 10 \text{ V}$ , $V_{GS} = 4.5 \text{ V}$ , $I_D = 20 \text{ A}$		45	65	
Gate-Drain Charge	$Q_{gd}$			16		
Gate Resistance	$R_g$			13		
Turn-On Delay Time	$t_{d(on)}$			0.2	1.1	Ω
Rise Time	$t_r$	$V_{DD} = 10 \text{ V}$ , $R_L = 1 \Omega$ $I_D \geq 10 \text{ A}$ , $V_{GEN} = 4.5 \text{ V}$ , $R_g = 1 \Omega$			45	ns
Turn-Off Delay Time	$t_{d(off)}$				35	
Fall Time	$t_f$				60	
Turn-On Delay Time	$t_{d(on)}$				90	
Rise Time	$t_r$	$V_{DD} = 10 \text{ V}$ , $R_L = 1 \Omega$ $I_D \geq 10 \text{ A}$ , $V_{GEN} = 10 \text{ V}$ , $R_g = 1 \Omega$			30	ns
Turn-Off Delay Time	$t_{d(off)}$				20	
Fall Time	$t_f$				10	
					30	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25^\circ\text{C}$			60	A
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$				100	
Body Diode Voltage	$V_{SD}$	$I_S = 10 \text{ A}$		0.8	1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 10 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $T_J = 25^\circ\text{C}$		60	90	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			75	115	
Reverse Recovery Fall Time	$t_a$			27		ns
Reverse Recovery Rise Time	$t_b$			33		

Notes:

- a. Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

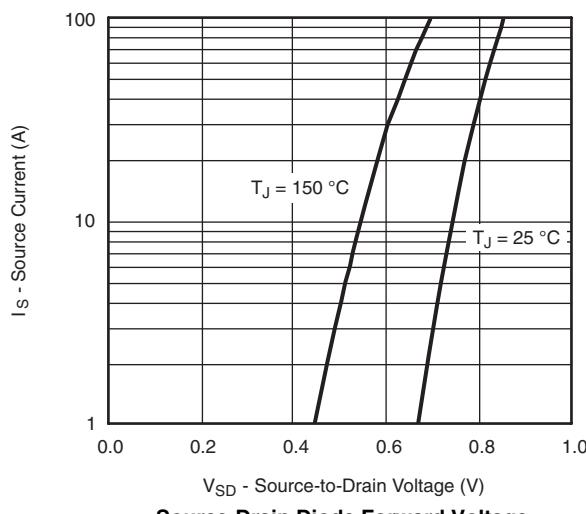
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted


## SiE874DF

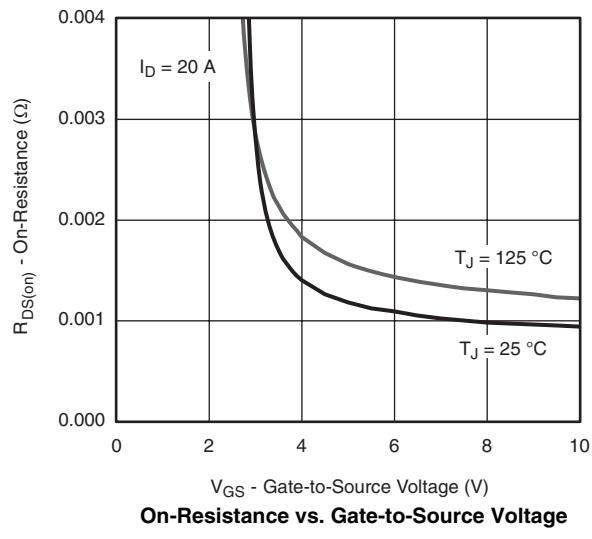
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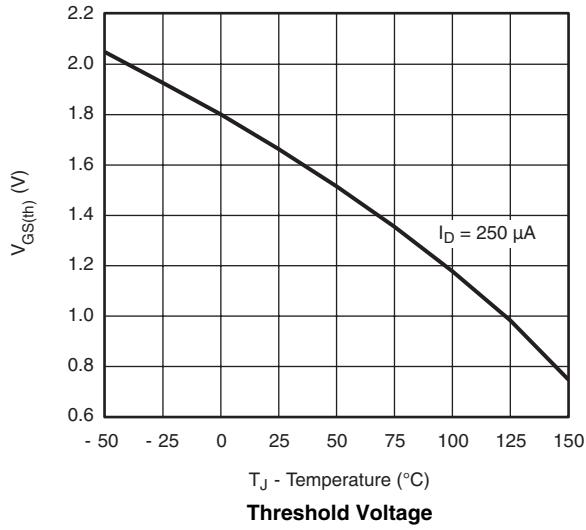
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



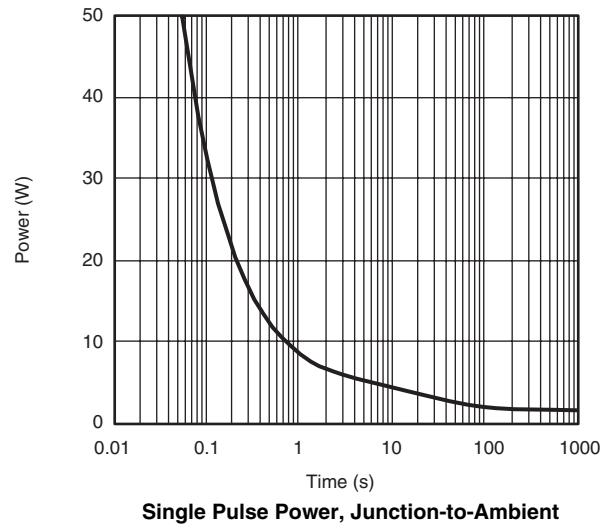
Source-Drain Diode Forward Voltage



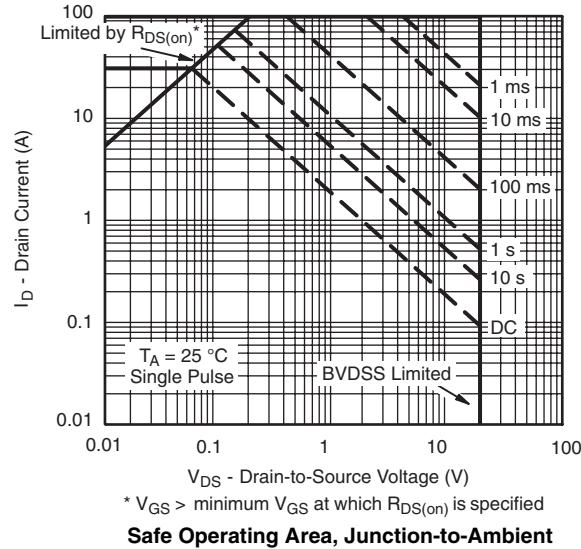
On-Resistance vs. Gate-to-Source Voltage



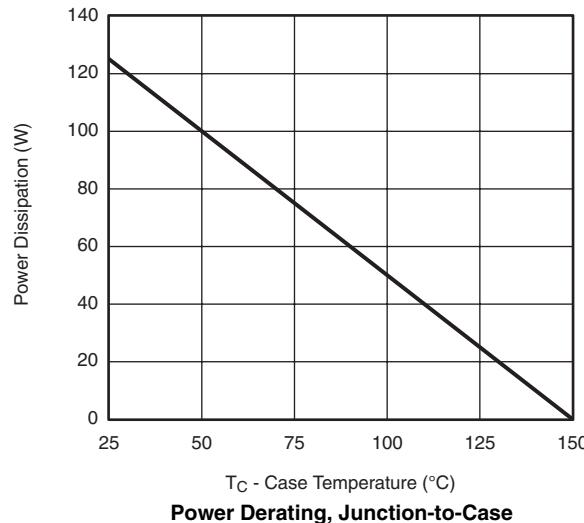
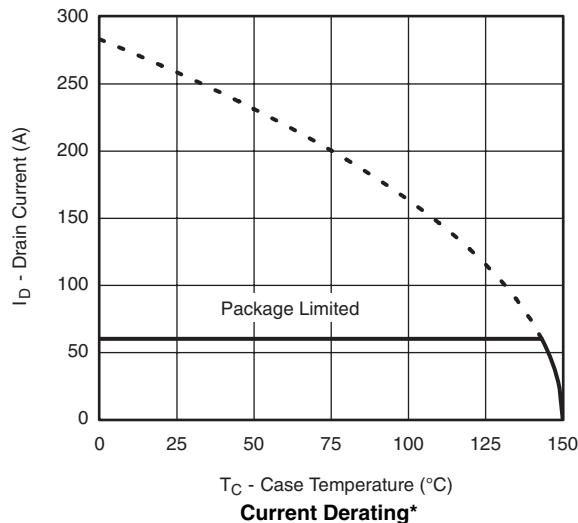
Threshold Voltage



Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted


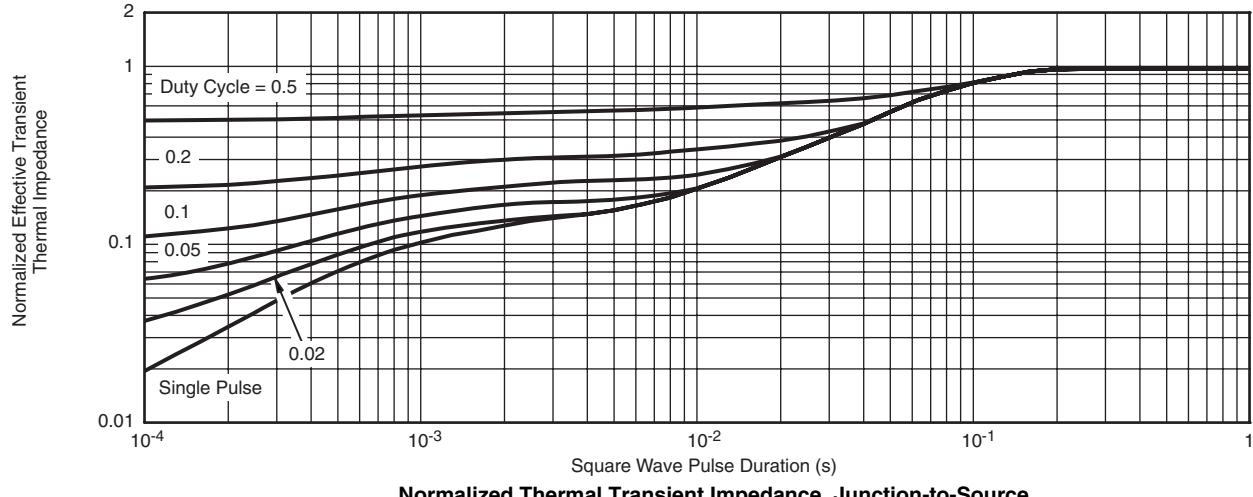
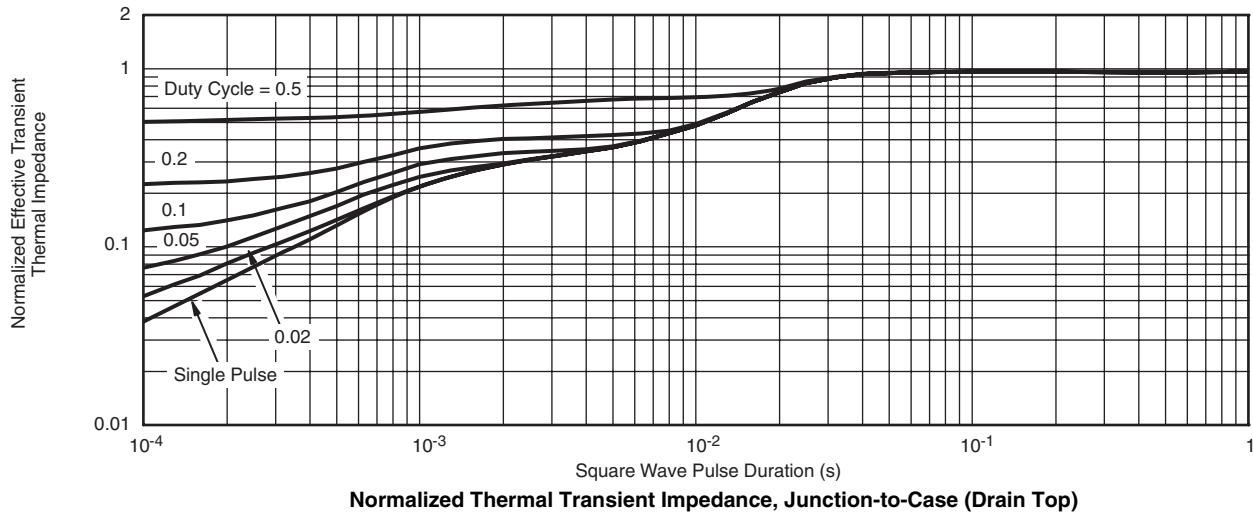
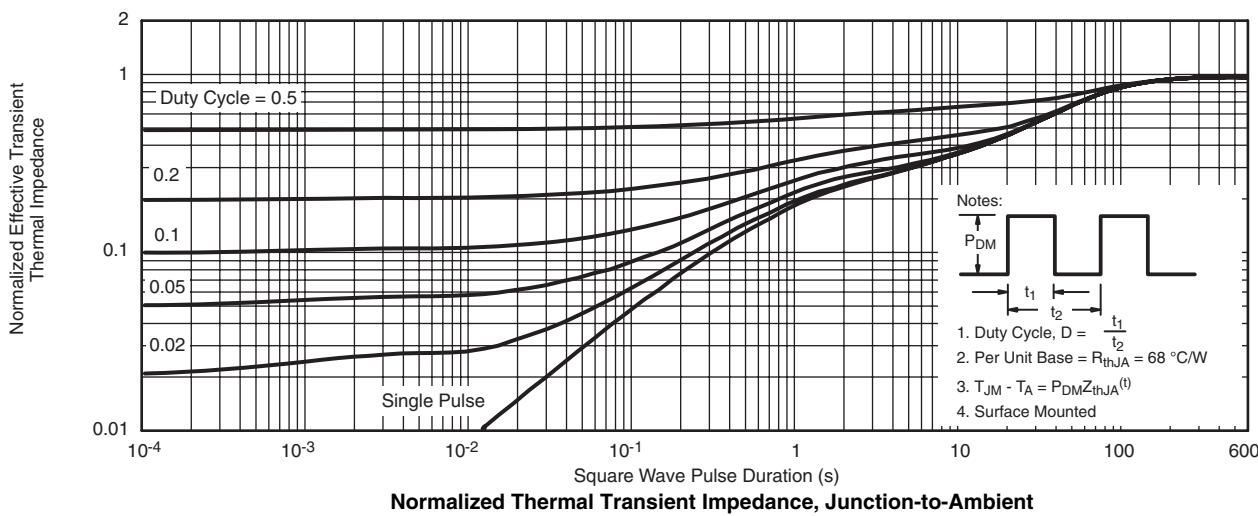
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?65350](http://www.vishay.com/ppg?65350).

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